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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 19

Application Number: 09/394,302
Filing Date: September 10, 1999
Appellant(s): DEAN ET AL.

Frederick W. Gibb, III
Reg. No. 37,629
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 24 March 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because appellant merely points out differences in what the claims cover (MPEP §1.192 (c)(7)). As the arguments presented by appellant address both independent claims, claims are grouped as one group.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

4291404	Steiner	9-1981
6452411	Miller et al.	9-2002
6499121	Roy et al.	12-2002

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 55-70 are rejected under 35 U.S.C. §103.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 55-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. Referring to claim 55, Steiner discloses a transportable circuit chip test device comprising: a transportable test box (See figure 1.); a test board in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated..."), wherein said test board comprises: a socket adapted to hold integrated circuit chips to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.). Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one

integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

Referring to claim 56, Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing procedures can identify the particular input/output combination for which the unit under

test failed to respond properly if this is considered important to the user.").

Referring to claim 57, Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated...").

Referring to claim 58, Steiner in combination with Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

Referring to claim 59, Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

Referring to claim 60, Steiner in combination with Miller et al. disclose each of said test boards includes comparators electrically connected to said sockets (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Referring to claim 61, Steiner in combination with Miller et al. disclose said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)."), and wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Referring to claim 62, Steiner in combination with Miller et al. disclose said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously (From the technical field of Miller et al., "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel.").

Referring to claim 63, Steiner discloses a transportable integrated circuit (IC) chip test device, said device comprising: a transportable test box (See figure 1.); a test board mounted in said test box (See figure 2.); and a portable power supply in said test box

connected to said test boards (From the abstract, "A battery operated..."), wherein said test board comprises: sockets adapted to hold an IC chip to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.). Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time". Further, although Steiner does not specifically disclose the comparison of a plurality of ICs, it is known in the art. An example of this is further shown by Miller et al. Miller et al. disclose said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said IC chips simultaneously, and wherein said testing circuitry identifies a defective IC chip as one having a different output when compared to outputs of the other ASIC chips, when all IC chips are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of

a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from the technical field, "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel." Wherein a faulty circuit's output is different.). A person of ordinary skill in the art at the time of the invention would have been motivated to compare DUTs in a portable tester because, from line 24 of column 1, "the manufacturer expects each constituent IC device to be virtually free of defects and to perform according to its specifications." Further, although Steiner does not specifically disclose the test device is adapted to test application specific integrated circuits (ASICs), the testing of ICs that are application specific is well known in the art. An example of this is an ASIC tester. A person of ordinary skill in the art at the time of the invention would have been motivated to test ASICs because they can be faulty.

Referring to claim 64, Steiner in combination with Miller et al. disclose all of said ASIC chips have an identical design (From line 6 of column 3, "As briefly summarized above, an embodiment of the invention provides for more efficient testing of a number of similar, and preferably identical, IC devices in parallel without altering the test program or the conventional tester.").

Referring to claim 65, Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

Referring to claim 66, Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated...").

Referring to claim 67, Steiner in combination with Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not

shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

Referring to claim 68, Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

Referring to claim 69, Steiner in combination with Miller et al. disclose all of said comparators are connected to known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs). The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. as applied to claim 63 above, and further in view of US 6499121 to Roy et al. Referring to claim 70, although Steiner in combination with Miller et al. do not specifically disclose by comparing whether

outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested, testing without a known output is known in the art. An example of this is given by Roy et al. in line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs. In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the

interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT and within-DUT comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." A person of ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into a portable circuit tester because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

Further, the rejection of record is herein presented a result of facts found in the prior art:

1. Steiner discloses a transportable circuit chip test device comprising: a transportable test box (See figure 1.).

2. Steiner discloses a test board in said test box (See figure 2.).

3. Steiner discloses a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated...").

4. Steiner discloses said test board comprises: a socket adapted to hold integrated circuit chips to be tested while being transported (See figure 1, element 10.).

5. Steiner discloses testing circuitry electrically connected to said sockets (See figure 2, element 25.).

6. Miller et al. disclose the testing of more than one integrated circuit in a system (From the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels.").

7. Miller et al. disclose it is advantageous to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

8. Steiner discloses visual test failure indicators, such that said visual test failure indicators is adjacent to said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the

test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

9. Steiner discloses the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated...").

10. Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

11. Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

12. Miller et al. disclose each of said test boards includes comparators electrically connected to said sockets (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from

the corresponding locations in the DUTs and expected responses obtained form the KGD.").

13. Miller et al. disclose said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)."), and wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

14. Miller et al. disclose said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously (From the technical field of Miller et al., "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel.").

15. Miller et al. disclose said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests

all of said IC chips simultaneously, and wherein said testing circuitry identifies a defective IC chip as one having a different output when compared to outputs of the other ASIC chips, when all IC chips are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from the technical field, "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel." Wherein a faulty circuit's output is different.).

16. Miler et al. disclose it would be advantageous to compare DUTs in a portable tester because, from line 24 of column 1, "the manufacturer expects each constituent IC device to be virtually free of defects and to perform according to its specifications."

17. Wherein the testing of integrated circuits has already been shown (fact 1), the testing of ICs that are application specific is well known in the art. An example of this is an ASIC tester.

18. Miller et al. disclose all of said ASIC chips have an identical design (From line 6 of column 3, "As briefly summarized above, an embodiment of the invention provides for more efficient testing of a number of similar, and preferably identical, IC devices in

parallel without altering the test program or the conventional tester.").

19. Miller et al. disclose all of said comparators are connected to known good integrated circuit chip such that any IC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective IC chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs). The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

20. Roy et al. disclose testing circuitry does not require a specific proper output that a given input should produce for the specific design of IC chip being tested (From line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs. In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry may be further enhanced with error detection capability based on the

responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT and within-DUT comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

21. Roy et al. disclose it would be advantageous to test without requiring a specific proper output that a given input should produce for the specific design of IC chip being tested because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

In regard to claim 55, Steiner in view of Miller et al. discloses every claimed limitation as set forth in findings 1-7.

In regard to claim 56, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 8.

In regard to claim 57, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 9.

In regard to claim 58, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 10.

In regard to claim 59, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 11.

In regard to claim 60, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 12.

In regard to claim 61, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 13.

In regard to claim 62, Steiner in view of Miller et al. discloses every claimed

limitation as set forth in finding 14.

In regard to claim 63, Steiner in view of Miller et al. discloses every claimed limitation as set forth in findings 1-7 and 15-17.

In regard to claim 64, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 18.

In regard to claim 65, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 8.

In regard to claim 66, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 9.

In regard to claim 67, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 10.

In regard to claim 68, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 11.

In regard to claim 69, Steiner in view of Miller et al. discloses every claimed limitation as set forth in finding 19.

In regard to claim 70, Steiner in view of Miller et al. in further view of Roy et al. discloses every claimed limitation as set forth in findings 20 and 21.

(11) Response to Argument

Group I. Appellant argues the invention is designed to test IC chips while they are being transported. Examiner has interpreted testing while transporting as functional language. While a functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the

art, if the prior art fails to explicitly disclose the limitation recited as functional language, the prior art must then disclose all claimed structural limitations and that disclosed structure must be inherently capable of performing the recited function. The structure of the apparatus described by Appellant has been shown by Examiner (see facts 1-7 and 15-17). The claimed functionality of testing while transporting the apparatus is inherent to the device as disclosed by at least Steiner in fact 1. Steiner has disclosed a portable circuit testing device, wherein such a device is inherently transportable, e.g., capable of being placed in a means of transportation. Fact 1, the figure of a portable circuit tester, clearly indicates that the device is of such a nature that transportation would be rendered an inherent property of portability and would only rely on a person of ordinary skill in the art, or no skill, to place in a conveyance. While functional language must be evaluated and considered for what it fairly conveys to a person of ordinary skill in the art, a recitation of function may not distinguish over the prior art since an apparatus claim covers what a device is, not what a device does, as well decided by the Federal Circuit and set forth in MPEP 2114.

Further with regards to this argument, Appellant has not even shown that testing occurs. From the independent claims, the language clearly shows that the test device is "adapted to hold integrated circuit chips to be tested", an intended use. Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation (MPEP 2106 II.C. paragraph 4). It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to

so perform. Examiner holds that the disclosure of the applied prior art is capable of performing in the claimed manner. Again, as per fact 1, the figure of a portable circuit tester clearly indicates that the device is of such a nature that transportation would be rendered an inherent property of portability and would only rely on a person of ordinary skill in the art, or no skill, to place in a conveyance.

Regarding Appellant's argument that the combination of Steiner with Roy/Miller to allow the testing of multiple chips in parallel destroys its ability to remain easily portable, Examiner has shown motivation to combine the teachings of the applied references. The matter of speculation as to whether it will remain "easily" portable has no bearing on its overall utility and at best only limits it by degrees.

Further, Examiner recognizes this as an argument against combination by citing bodily incorporation. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Examiner argues that, in general, when presented with a portable circuit tester and a circuit tester of undisclosed portability with additional circuit testing functionality, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate more circuit testing functionality into a portable circuit tester. Specific motivation for incorporation can be found in the rejection of paper no. 11.

Regarding Appellant's argument that there is no teaching of the transportable test box or a power supply within such a test box, Steiner has specifically shown a test box that is portable (fact 1) and that that test box is powered by a battery (fact 3). From page 15 of Appellant's Appeal Brief, Appellant has admitted, "Steiner only discloses a battery powered single chip test board..." Appellant further argues that this test box must "surround and protect" such a test board, but no such claim has been made to this effect.

Appellant's further argue that the dependent claims are patentable over prior art, but present no specific arguments as to why any one dependent claim would be allowable over the prior art and arguments of record. Appellant merely asserts patentability in light of the alleged patentability of independent claims.

For the above reasons, it is believed that the rejections should be sustained.

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gc
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